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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,608	08/21/2003	Charles E. Larson	108298502US2	9809
25096	7590	06/11/2004	EXAMINER	
PERKINS COIE LLP			TOLEDO, FERNANDO L	
PATENT-SEA			ART UNIT	
P.O. BOX 1247			PAPER NUMBER	
SEATTLE, WA 98111-1247			2823	

DATE MAILED: 06/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/646,608

Applicant(s)

LARSON ET AL.

Examiner

Fernando L. Toledo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 69-81 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 69-81 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20030821</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 69 – 76 and 78 – 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayraktaroglu (U. S. patent 5,496,755) in view of Bruel (U. S. patent 5,374,564).

In re claim 69, Bayraktaroglu in the U. S. patent 5,496,755; figures 1 – 4 and related text discloses a substrate having a first portion with a first surface, the first portion having first and second voids extending from the first surface to a separation plane, the first void tapered along a first axis and the second void tapered along a second axis generally parallel to the first axis, the first and second tapered voids being larger toward the separation line; and at least one operable microelectronic device disposed at least proximate to the first surface and between the first and second axes (Figure 4).

Bayraktaroglu does not show a second portion with a second surface opposite the first surface and a separation plane between the first and second portions.

However, Bruel in the U. S. patent 5,374,564; figures 1 – 4 and related text discloses an alternative method to form thin substrates without requiring an initial substrate of a different nature from that of the chosen semiconductor, without requiring very high implantation dosage,

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or an etch-stop, but which still makes possible to obtain a uniform, controlled thickness (Column 2, lines 5 – 13).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the substrate of Bayraktaroglu by having a larger substrate and then cutting through a predetermined separation line as taught by Bruel, since, it can be done without requiring an initial substrate of a different nature from that of the chosen semiconductor, without requiring very high implantation dosage, or an etch-stop, but which still makes possible to obtain a uniform, controlled thickness.

3. In re claim 70, Bayraktaroglu discloses wherein the microelectronic device is disposed in the first portion of the substrate between the first and second tapered voids (Figure 4).

4. In re claim 71, Bayraktaroglu in view of Bruel discloses wherein the first portion and the second portion have at least generally the same composition. (Column 2 of Bruel).

5. In re claim 72, Bayraktaroglu teaches wherein the first external surface is separated from the second external surface by about 150 microns or less (column 5).

6. In re claim 73, Bayraktaroglu teaches wherein the voids are etched voids (column 5).

7. In re claim 74, Bayraktaroglu teaches wherein the first portion further includes a third void extending from the first surface to the separation plane, and wherein the first, second and third voids are regularly spaced apart from each other (figure 4 and claim 4).

8. In re claim 75, Bayraktaroglu discloses wherein the first portion further includes a third void extending from the first surface to the separation plane, and wherein the first, second and third voids are randomly spaced apart from each other (figure 4 and claim 4).

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9. In re claim 76, Bayraktaroglu discloses wherein the first and second voids each include a first end proximate to the first surface, and wherein the first ends are filled with a filler material (figure 4).

10. In re claim 78, Bayraktaroglu discloses further including a film layer disposed on the first surface (figure 4).

11. In re claim 79, Bayraktaroglu discloses wherein the film layer has an external surface facing an opposite direction from the second surface of the second portion, and wherein a distance between the external surface and the separation plane is less than approximately 150 microns (column 3).

12. In re claim 80, Bayraktaroglu discloses wherein the first and second voids have a conical configuration (figure 4).

13. In re claim 81, Bayraktaroglu discloses wherein the first void has a first depth and the second void has a second depth at least approximately equal to the first depth (figure 4).

14. Claim 77 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayraktaroglu in view of Bruel as applied to claims 69 – 76 and 78 – 81 above, and further in view of Wolf and Tauber (Silicon Processing for the VLSI Era Volume 1: Process Technology).

Bayraktaroglu in view of Bruel does not disclose wherein the semiconductor substrate is made of silicon.

However, Wolf, in the textbook, Silicon Processing for the VLSI Era Volume 1: Process Technology, page 1, discloses that silicon is the most important semiconductor material for the electronics industry among its advantages is that is readily available and therefore cheap compared to other semiconductor materials (page 1).

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It would have been obvious to one having ordinary skill in the art at the time the invention was made to use silicon to form the substrate of Bayraktaroglu since, as taught by Wolf, silicon is the most important semiconductor material for the electronics industry among its advantages is that is readily available and therefore cheap compared to other semiconductor materials.

Conclusion

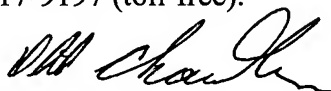
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



FToledo



Olik Chaudhuri
Supervisory Primary Examiner
Art Unit 2823